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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,850	12/18/2001	Shunpei Yamazaki	07977-188002/US3427/3434D	8129

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EXAMINER

COLEMAN, WILLIAM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/024,850

Applicant(s)

YAMAZAKI ET AL.

Examiner

W. David Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/951,819.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki, U.S. Patent 6,207,969 B1.
4. Pertaining to claim 1, Yamazaki discloses a semiconductor device having at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer formed over a substrate, said semiconductor layer having source and drain regions and a channel formation region interposed therebetween; and a gate electrode formed adjacent to said semiconductor layer, wherein said semiconductor layer comprises crystals arranged in a direction substantially parallel with a length direction of said channel formation region, wherein a standard deviation of S-value of said thin film transistor is within 10 mV/dec for an N-channel type and 15 mV/dec for a P-channel type (see Table 1, S-values).
5. Pertaining to claim 2, Yamazaki discloses a semiconductor device according to claim 1, wherein said semiconductor layer contains a metal element for promoting crystallization at a

concentration of not higher than 1×10^{18} atoms/cm³ (this concentration is disclosed in column 4, lines 57, where Yamazaki discloses the concentration Japanese Unexamined Patent Publication Hei. 07-321339).

6. Pertaining to claim 3, Yamazaki discloses a semiconductor device according to claim 1, wherein said semiconductor device is incorporated into an electronic apparatus selected from the group consisting of a TV camera, a head mounted display, a car navigation, a portable telephone, a video camera and a projector (see **FIGS. 15A-15E**).

7. Pertaining to claim 4, Yamazaki discloses a semiconductor device having at least one thin film transistor, said thin film transistor comprising: a semiconductor layer formed over a substrate, said semiconductor layer having source and drain regions and a channel formation region interposed therebetween; and a gate electrode formed adjacent to said semiconductor layer, wherein said semiconductor layer comprises crystals arranged in a direction substantially parallel with a length direction of said channel formation region, wherein a length of said channel formation region is 0.01 to 2 μm (please see **FIGS. 5A-9B** for the channel formation region and column 10, lines 17-19 for the teaching of reducing the channel length to effectively reduce the S-value as claimed and disclosed in Table 1).

8. Pertaining to claim 5, Yamazaki teaches a semiconductor device according to claim 4, wherein said semiconductor layer contains a metal element for promoting crystallization at a concentration of not higher than 1×10^{18} atoms/cm³.

9. Pertaining to claim 6, Yamazaki teaches a semiconductor device according to claim 4, wherein said semiconductor device is incorporated into an electronic apparatus selected from the

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group consisting of a TV camera, a head mounted display, a car navigation, a portable telephone, a video camera and a projector.

10. Pertaining to claim 7, Yamazaki teaches a semiconductor device having at least one thin film transistor, said thin film transistor comprising: a semiconductor layer formed over a substrate, said semiconductor layer having source and drain regions and a channel formation region interposed therebetween; and a gate electrode formed adjacent to said semiconductor layer, wherein said semiconductor layer comprises crystals arranged in a direction substantially parallel with a carrier flow direction between said source and drain regions, wherein a standard deviation of S-value of said thin film transistor is within 10 mV/dec for an N-channel type and 15 mV/dec for a P-channel type.

11. Pertaining to claim 8, Yamazaki teaches a semiconductor device according to claim 7, wherein said semiconductor layer contains a metal element for promoting crystallization at a concentration of not higher than 1×10^{18} atoms /CM³.

12. Pertaining to claim 9, Yamazaki teaches a semiconductor device according to claim 7, wherein said semiconductor device is incorporated into an electronic apparatus selected from the group consisting of a TV camera, a head mounted display, a car navigation, a portable telephone, a video camera and a projector.

13. Pertaining to claim 10, Yamazaki teaches a semiconductor device having at least one thin film transistor, said thin film transistor comprising: a semiconductor layer formed over a substrate, said semiconductor layer having source and drain regions and a channel formation region interposed therebetween; and a gate electrode formed adjacent to said semiconductor layer, wherein said semiconductor layer comprises crystals arranged in a direction substantially

parallel with a carrier flow direction between said source and drain regions, wherein a length of said channel formation region is 0.01 to 2 μm .

14. Pertaining to claim 11, Yamazaki teaches a semiconductor device according to claim 10, wherein said semiconductor layer contains a metal element for promoting crystallization at a concentration of not higher than 1×10^{18} atoms / cm^3 .

15. Pertaining to claim 12, Yamazaki teaches a semiconductor device according to claim 10, wherein said semiconductor device is incorporated into an electronic apparatus selected from the group consisting of a TV camera, a head mounted display, a car navigation, a portable telephone, a video camera and a projector.

16. Pertaining to claim 13, Yamazaki teaches an active matrix display device comprising: a pixel matrix circuit formed over a substrate; a logic circuit formed over said substrate, said logic circuit having thin film transistors, wherein each of said thin film transistors comprises: a semiconductor layer formed over a substrate, said semiconductor layer having source and drain regions and a channel formation region interposed therebetween; and a gate electrode formed adjacent to said semiconductor layer, wherein said semiconductor layer comprises crystals arranged in a direction substantially parallel with a length direction of said channel formation region, wherein a standard deviation of S-value of said thin film transistor is within 10 mV/dec for an N-channel type and 15 mV/dec for a P-channel type.

17. Pertaining to claim 14, Yamazaki teaches an active matrix display device according to claim 13, wherein said semiconductor layer contains a metal element for promoting crystallization at a concentration of not higher than 1×10^{18} atoms / cm^3 .

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18. Pertaining to claim 15, Yamazaki teaches an active matrix display device according to claim 13, wherein said semiconductor device is incorporated into an electronic apparatus selected from the group consisting of a TV camera, a head mounted display, a car navigation, a portable telephone, a video camera and a projector.

19. Pertaining to claim 16, Yamazaki teaches an active matrix display device comprising: a pixel matrix circuit formed over a substrate; a logic circuit formed over said substrate, said logic circuit having thin film transistors, wherein each of said thin film transistors comprises: a semiconductor layer formed over a substrate, said semiconductor layer having source and drain regions and a channel formation region interposed therebetween; and a gate electrode formed adjacent to said semiconductor layer, wherein said semiconductor layer comprises crystals arranged in a direction substantially parallel with a carrier flow direction between said source and drain regions, wherein a standard deviation of S-value of said thin film transistor is within 10 mV/dec for an N-channel type and 15 mV/dec for a P-channel type.

20. Pertaining to claim 17, Yamazaki teaches an active matrix display device according to claim 16, wherein said semiconductor layer contains a metal element for promoting crystallization at a concentration of not higher than 1×10^{18} atoms/cm³.

21. Pertaining to claim 18, Yamazaki teaches an active matrix display device according to claim 16, wherein said semiconductor device is incorporated into an electronic apparatus selected from the group consisting of a TV camera, a head mounted display, a car navigation, a portable telephone, a video camera and a projector.

Double Patenting

22. Claims 1-18 are directed to the same invention as that of claims 1, 5, 6, 11, 15 and 15 of commonly assigned U.S. Patent 6,365,933 B1. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

23. Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

24. Failure to comply with this requirement will result in a holding of abandonment of this application.

Conclusion

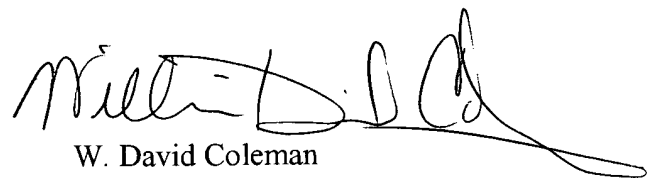
25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the

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organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink, appearing to read 'W. David Coleman', with a long horizontal flourish extending to the right.

W. David Coleman
Primary Examiner
Art Unit 2823

WDC
June 27, 2003